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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,358	02/29/2000	Philip A Bourekas	M-7949US	1167

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EXAMINER
HUYNH, KIM T

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2189	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/515,358	BOUREKAS, PHILIP A	
	Examiner	Art Unit	
	Kim Huynh	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8, 10-15 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2- 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US Patent 6,425,039) in view of Worley, Jr. et al. (US Patent 5,596,733)

a. As per claim 2, Yoshioka ('039) discloses a processor comprises

- a set of general purpose registers; (fig.3, 31) (col.8, lines 62-67)
- a set of exception registers (col.5, lines 33-42) . (col.13, lines 63-67), (col.14, lines 1-13),

Yoshioka discloses the limitation as above except Yoshioka fails to disclose exception registers that are switched for general purpose registers when an exception occurs; however, Worley discloses a set of exception registers (fig.2, 106) , (col.8, lines 41-51) wherein if such an exception occurred, the selects the default value for the exception from the storage table 176, (col.10, lines 23-33)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Worley's teaching into Yoshioka 's method to have a set of dedicated exception registers wherein switched for a subset of set of general purpose registers when exception occurs so as to

be advantage to response to an instruction which already have a fix-up instructions just wait for the substitution. (col.5, lines 37-45)

b. As per claim 3, Yoshioka ('039) discloses set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low priority. *(col.13, lines 12-42), wherein priority exception events be assigned)*

c. As per claim 4, Yoshioka ('039) discloses processor provides a dedicated vector to said set of exception registers for said exception. (col.13, lines 63-67), (col.14, lines 1-13),

d. As per claim 5, Yoshioka ('039) discloses the limitations as discussed as above which show multiple exception registers. However, Yoshioka fails to show eight exception registers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the additions of more registers, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

e. As per claim 6, Yoshioka ('039) discloses a portion of said set of exception registers is for set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls. (col.4, lines 20-28)

f. As per claim 7, Yoshioka ('039) discloses processor provides a first dedicated vector to software which uses said portion of said set of exception registers for interrupts and a second dedicated vector to software which uses said another

portion of said set of exception registers for servicing operating systems calls. (col.3, lines 6-47), (col.4,lines 20-28)

g. As per claim 8, Yoshioka ('039) fails to discloses a select logic circuit having a first input that receives an exception register active bit and a second input that receives a register address bit, said select logic circuit provides an output signal on an output used to select between said set of general purpose registers and said exception registers. However, Worley discloses functional unit (fig.2, 40) performs operations to execute the instruction and select registers between exception register (58) and general register (52) , (col.6, lines 31-58)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Worley's teaching into Yoshioka 's method to have a logic circuit to select and switch between the two set of registers, the exception and general registers so as to be advantage to response to an instruction which already have a fix-up instructions just wait for the substitution. (col.5, lines 37-45)

h. As per claims 20, 21, 24 Yoshioka ('039) discloses a processor comprising:

- a set of general purpose registers; (fig.3, 31) (col.8, lines 62-67)
- predetermined priority level is detected by processor whether or not switched when exception having a priority less than the predetermined priority level is detected by said processor. (col.5, lines 16-22)

Yoshioka discloses the limitation as above except Yoshioka fails to disclose dedicated exception registers that are switched for general purpose

registers when an exception occurs; however, Worley discloses a set of exception registers (fig.2, 106) , (col.8, lines 41-51) wherein if such an exception occurred, the selects the default value for the exception from the storage table 176, (col.10, lines 23-33)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Worley's teaching into Yoshioka 's method to have a set of dedicated exception registers wherein switched for a subset of set of general purpose registers when exception occurs so as to be advantage to response to an instruction which already have a fix-up instructions just wait for the substitution. (col.5, lines 37-45)

i. As per claim 22, Yoshioka fails to discloses a select logic circuit having a first input that receives an exception register active bit and a second input that receives a register address bit, said select logic circuit provides an output signal on an output used to select between said set of general purpose registers and said exception registers. However, Morley discloses functional unit (fig.2, 40) performs operations to execute the instruction and select registers between exception register (58) and general register (52) , (col.6, lines 31-58)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Worley's teaching into Yoshioka 's method to have a logic circuit to select and switch between the two set of registers, the exception and general registers so as to be advantage to

response to an instruction which already have a fix-up instructions just wait for the substitution. (col.5, lines 37-45)

j. As per claim 23, Yoshioka ('039) discloses a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls. (col.4, lines 20-28)

3. Claim 10-12, 13-15, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US Patent 6,038,661) in view of Worley, Jr. et al. (US Patent 5,596,733)

a. As per claim 12, Yoshioka ('661) discloses a method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

- servicing said exception using said at least one set of exception registers if said exception is a high priority exception; (col.13, lines 1-8)
- preserving information in the set of general purpose registers in a memory if said exception is a low priority exception; (col.9, lines 48-52)

Yoshioka discloses the limitation as above except Yoshioka fails to disclose swapping a set of general purpose registers for exception registers if an exception is a high priority exception and swapping out exception register and resuming execution of task if exception is high priority. However Worley discloses a set of exception registers (fig.2, 106) , (col.8, lines 41-51) wherein if such an exception occurred, the selects the default value for the exception

from the storage table 176, (col.10, lines 23-33) and if an exception produced assigned priority. (col.9, lines 50-54)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Worley's teaching into Yoshioka 's method to swapping a set of general purpose registers for exception registers if an exception is a high priority exception and swapping out exception register and resuming execution of task if exception is high priority. so as to be advantage to response to an instruction which already have a fix-up instructions just wait for the substitution. (col.5, lines 37-45)

b. As per claim 10, at least one set of exception registers is a dedicated set of exception registers. (col.8, lines 62-66)

c. As per claim 11, Yoshioka ('661) servicing exception using at least one set of exception registers comprises modifying the values of the registers in set of exception registers without disrupting the state of the interrupted task (col.23, lines 3-21), (col.25, lines 38-46)

d. As per claims 14, 19 Yoshioka ('661) discloses exception is a high priority exception and is either an interrupt or an operating system call, said method further comprising:

- Providing a first vector and activating at least one set of exception registers for high priority exception (col.22, lines 46-60), (col.19, lines 47-65) ,(col.17, lines 60-67), (col.18, lines 1-5), (col.13, lines 1-8), wherein

predetermine priority vector has assigned depend on the exception events occurs by software implementation)

- Providing a second vector and not activating set of exception registers for lower priority exceptions. (col.22, lines 46-60) (col.17, lines 60-67), (col.18, lines 1-5), (col.13, lines 1-8), wherein predetermine priority vector has assigned depend on the exception events occurs by software implementation)
- Providing a third vector and not activating said set of exception registers for lower priority exceptions. (col.17, lines 60-67), (col.18, lines 1-5), (col.13, lines 1-8), wherein predetermine priority vector has assigned depend on the exception events occurs by software implementation)

e. As per claim 13, Yoshioka ('661) discloses first vector is a dedicated vector and said providing said first vector automatically separates said high priority exception from said lower priority exceptions. (col.3, lines 26-47), (col.13, lines 1-8), wherein, vector predetermined and priority level had been defined, therefore high and low priority has already separates)

f. As per claim 15, Yoshioka ('661) discloses first vector and said second vector are dedicated vectors and said providing said first vector and providing said second vector automatically separates said high priority exception from said lower priority exceptions. (col.3, lines 26-47), (col.13, lines 1-8), wherein, vector predetermined and priority level had been defined, therefore high and low priority has already separates)

g. As per claim 17, Yoshioka ('661) discloses an apparatus for executing tasks and servicing exceptions, said apparatus comprising:

- means for interrupting a task when an exception is asserted; (col.22, lines 46-60), wherein specified by description of vector)
- means for servicing said exception without disrupting the state of the interrupted task, including means for activating at least one set of dedicated exception registers; (col.24, lines 63-67), (col.25, lines 17-37), (col.10, lines 12-20)
- means for resuming executing of said interrupted task, including means for deactivating said dedicated exception registers and activating general purpose registers to resume execution of said task. (col.10, lines 27-33)

h. As per claim 18, Yoshioka ('661) fails to discloses a select logic circuit having a first input that receives an exception register active bit and a second input that receives a register address bit, said select logic circuit provides an output signal on an output used to select between said set of general purpose registers and said exception registers. However, Worley discloses functional unit (fig.2, 40) performs operations to execute the instruction and select registers between exception register (58) and general register (52) , (col.6, lines 31-58)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Worley's teaching into Yoshioka 's method to have a logic circuit to select and switch between the two set of registers, the exception and general registers so as to be advantage to

response to an instruction which already have a fix-up instructions just wait for the substitution. (col.5, lines 37-45)

Response to Arguments

4. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

March 18, 2003

RUPAL DHARIA
PRIMARY EXAMINER